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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	197226US-2TTC
First Inventor or Application Identifier	NOBORU MATSUDA
Title	POWER MOS TRANSISTOR HAVING TRENCH GATE

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

1. ■ **Fee Transmittal Form (e.g. PTO/SB/17)** **(Submit an original and a duplicate for fee processing)**
2. ■ **Specification** **Total Pages** 19
3. ■ **Drawing(s) *(35 U.S.C. 113)* Total Sheets (Formal)** 7
4. □ Oath or Declaration Total Pages
   a. □ Newly executed (original or copy)
   b. □ Copy from a prior application *(37 C.F.R. §1.63(d))* *(for continuation/divisional with box 15 completed)*
      i. □ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see *37 C.F.R. §1.63(d)(2) and 1.33(b).*
5. □ Incorporation By Reference *(usable if box 4B is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4B, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

ACCOMPANYING APPLICATION PARTS

6. □ **Assignment Papers (cover sheet & document(s))**
7. □ 37 C.F.R. §3.73(b) Statement *(when there is an assignee)* □ Power of Attorney
8. □ English Translation Document *(if applicable)*
9. ■ **Information Disclosure Statement (IDS)/PTO-1449** □ **References (1)**
10. □ Preliminary Amendment
11. ■ **White Advance Serial No. Postcard**
12. □ Small Entity Statement(s) □ Statement filed in prior application. Status still proper and desired.
13. ■ **Certified Copy of Priority Document(s) (1)** ***(if foreign priority is claimed)***
14. ■ **Other:** **REQUEST FOR PRIORITY**
    LIST OF INVENTORS' NAMES...

15. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below:*
    □ Continuation □ Divisional □ Continuation-in-part (CIP) of prior application no.:
    Prior application information: Examiner: Group Art Unit:

16. Amend the specification by inserting before the first line the sentence:
    □ This application is a □ Continuation □ Division □ Continuation-in-part (CIP) of application Serial No. Filed on
    □ This application claims priority of provisional application Serial No. Filed

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Docket No. **197226US2TTC**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR(S) **NOBORU MATSUDA ET AL**

SERIAL NO: **New Application**

FILING DATE: **Herewith**

FOR: **POWER MOS TRANSISTOR HAVING TRENCH GATE**

FEE TRANSMITTAL

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FOR	NUMBER FILED	NUMBER EXTRA	RATE	CALCULATIONS
TOTAL CLAIMS	20 - 20 =	0	× $18 =	$0.00
INDEPENDENT CLAIMS	4 - 3 =	1	× $78 =	$78.00
☐ MULTIPLE DEPENDENT CLAIMS (If applicable)			+ $260 =	$0.00
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197226US-2TTC

TITLE OF THE INVENTION

POWER MOS TRANSISTOR HAVING TRENCH GATE

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims benefit of priority under 35 U.S.C. 119 to Japanese Patent Application No. P11-269922 filed September 24, 1999, the entire contents of which are incorporated by reference herein.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a structure of a power MOS transistor having a trench gate.

Discussion of the Background

Fig. 1 is a plan view showing a spline-structured MOS transistor manufactured based on current product design rules. Trench gates 45 and source contacts 46 are alternately formed on a semiconductor substrate. Each of the source contacts 46 is connected to a source electrode formed on a layer formed further thereon.

Fig. 2 is an upper surface view showing a pattern of an offset mesh-structured MOS transistor manufactured based on current product design rules. Trench gates 38 and source contacts 44 are alternately formed on a semiconductor substrate. Each of the source contacts 44 is connected to a source electrode formed on a layer formed further thereon. The offset mesh type is designed to realize a high degree of integration by

forming transistors in longitudinal and lateral directions. In this MOSFET, an arraying ratio of the trench gates 38 and the source contacts 44 is set at 1:1. In other words, one trench gate and one source contact constitute one MOSFET.

Fig. 3 is a detailed sectional view of the MOS transistor shown in Fig. 2, taken along the lines 6-6 shown in Fig. 2. Now, the structure of this section will be described, as well as a method of manufacturing a semiconductor device including such structure.

First, as shown in Fig. 3, an N-type epitaxial layer 32 is formed on, for example an N+ type semiconductor substrate 31. On the surface of this epitaxial layer 32, a double diffused layer composed of a P-type base diffused layer 33 and an N+ type source diffused layer 34 is formed. Then, after an SiO film is formed on the source diffused layer 34, the resultant structure is subjected to patterning by a resist. Using this as a mask, the SiO film is punched. The resist is removed, and then using the SiO film as a mask, a trench 35 is formed to a depth punching through the base diffused layer 33. Subsequently, a gate insulating film 36 is formed on a full surface, and a polysilicon film 37 for a gate electrode is formed on the gate insulating film 36. Then, the polysilicon film 37 is removed until the surface of the gate insulating film 36 is exposed, and a trench gate 38 is formed.

Subsequently, to separate the trench gate 38 from the source contact, an interlayer film 39 is formed on a full surface. Using a resist (not shown) formed on the interlayer film 39 and then patterned, the interlayer film 39 is removed, and a contact hole 40 is formed to a depth punching through the source diffused layer 34. Then, impurity ions are implanted by using the interlayer film 39 as a mask, and a P+ type diffused layer 41 is formed in the bottom portion of the contact hole 40 inside the base diffused layer 33. Subsequently, a barrier metal layer 42 is formed on the full surface. An aluminum film 43 is formed on this barrier metal layer 42, and a source contact 44 is formed.

Fig. 4 is a sectional view showing a flow passage of a current when a voltage is applied to the MOS transistor shown in Fig. 3. When a drain voltage is applied to the semiconductor substrate 31, a channel region 45 is formed from the semiconductor substrate 31 to near the side face of the trench gate 38. A current flows from a drain through the channel region 45 to the diffused layer 34. The diffused layer 34 becomes a source region.

In this case, an increase in a channel density of the channel region 45 facilitates the flow of a current, making it possible to reduce the device resistance of the MOSFET.

Accordingly, to increase the number of channel regions 45, the number of trench gates 38, at the side faces of which channel regions 45 are formed, may be increased within a given region.

However, an increase in the number of trench gates 38 necessitates an increase in the number of source contacts 44. If a spacing between the trench gate 38 and the source contact 44 is small, shifting occurs in matching during a photo engraving process (PEP). An extra gate and source spacing must be provided for the trench gate 38 and the source contact 44. However, if an unexpected increase in the number of source pitches reduces the gate and source spacing, a reduction also occurs in the amount of margin between the gate and the source, resulting in a short-circuit failure therebetween.

Furthermore, if an opening of the source contact 44 is reduced, and the number of source pitches is increased in a given region, an aspect ratio of the contact hole 40 is increased, resulting in the impossibility of sufficient formation of the barrier metal layer 42 on the side face of the contact hole 40. The insufficient formation of the layer 42 causes reaction between the aluminum of the aluminum film 43 and the silicon of the substrate, which in turn generates aluminum spikes. Thus, because of improper formation of a depletion layer, current leakage occurs between the drain and the source.

SUMMARY OF THE INVENTION

The present invention was made to solve the foregoing problems, and it is an object of the invention to provide a semiconductor device having a trench gate, which is capable of increasing a channel region density and achieving low device resistance.

This and other objects are achieved according to the present invention by providing a novel semiconductor device including a first electrode gate group having a plurality of gate electrodes formed on a semiconductor substrate to be away from each other at first equal spacings; and a source contact having a portion formed separated from a first gate electrode of the first electrode gate group by a second spacing greater than the first spacing.

According to another aspect of the present invention, there is provided a semiconductor device including a first gate electrode group having a plurality of gate electrodes formed on a semiconductor substrate to be away from each other at first equal spacings; a source contact portion formed separated from the first gate electrode group to be away from the first gate electrode groups at a second spacing; and source regions for electrically interconnecting the first gate electrode group and the source contact, wherein the source regions are connected to each other at one end of the first gate electrode group, and separated from each other at the other end of the first gate electrode group.

According to a further aspect of the present invention, there is provided a semiconductor device including a first electrode gate group having a plurality of gate electrodes formed on a semiconductor substrate to be away from each other at first equal spacings; a second gate electrode group having a plurality of gate electrodes formed on the semiconductor substrate to be away from each other at the first equal spacings; a source contact portion formed between the first and second gate electrode groups to be away from the first and second gate electrode groups at a second spacing; and source regions for electrically interconnecting the first gate electrode group and the source contact portion. In

this case, the source regions are connected to each other at one end of the first gate electrode group, and separated from each other at the other end of the same. Preferably, the second spacing is greater than the first spacing.

Since the source regions are connected to each other at one end, and separated from each other at the other end, a channel density can be increased, making it possible to achieve low device resistance for the semiconductor device. In addition, since one source contact has a plurality of trench gates, the number of regions and an area between a source and a gate can be reduced.

In the semiconductor device of the invention, the source contact portion and the first gate electrode group constitute one MOS transistor. By combining MOS transistors having such configuration, low resistance and a high degree of integration can be achieved.

The semiconductor device of the invention further comprises a source electrode on the semiconductor substrate, and the source contact portion is an electrode drawn from a source electrode. Because of this drawn electrode, it is not necessary to form any source electrodes on the front face on the semiconductor substrate. Even if the source electrode is formed in a predetermined region, it can be drawn out, contributing to higher device integration.

Other objects, features, and advantages of the present invention will become apparent from the following detailed description. It should be understood, however, that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

A more complete appreciation of the present invention and many of its attendant advantages will be readily obtained by reference to the following detailed description considered in connection with the accompanying drawings, in which,

Fig. 1 is a plan view showing a pattern of a conventional line-structured MOS transistor;

Fig. 2 is a plan view showing a pattern of a conventional offset mesh-structured MOS transistor;

Fig. 3 is a sectional view showing a semiconductor device of a conventional technology, taken on line 6-6 of Fig. 2;

Fig. 4 is a sectional view showing a semiconductor device of a conventional technology, taken on line 6-6 of Fig. 2;

Fig. 5 is a plan view showing a pattern of a line-structured MOS transistor according to the invention;

Fig. 6 is a plan view showing a pattern of an offset mesh-structured MOS transistor according to the invention;

Fig. 7 is a sectional view showing a semiconductor device of the invention, taken on line 2-2 of Fig. 6;

Fig. 8 is a sectional view showing a semiconductor device having channel regions according to the invention;

Fig. 9 is a perspective view showing the semiconductor device having the channel regions according to the invention; and

Fig. 10 is an upper surface view showing a pattern of another offset mesh structure according to the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention relates to a structure of a power MOS transistor having a trench type gate electrode. The power MOS transistor is designed to obtain power by interconnecting a number of micro-pattern MOSFET cells in parallel. In general, the power MOS transistor is suited for a high-speed operation because of its fast switching speed. As regards its usage, this transistor is used for a switching power source, a motor control circuit, a wide-band power amplifier, and so on. The power MOS transistor is classified into a spline type and a mesh type, depending on the arrangements of trench gates and source contacts, and there is a difference in a degree of integration for the MOS transistor between these types. Configurations of the MOS transistors are nearly similar to each other.

Referring now to the drawings, where like reference numerals refer to the same or corresponding parts throughout the several views, and firstly referring to Figs. 5 and 6 thereof, the concept of the present invention is first described.

Fig. 5 is a plan view of the power MOS transistor of the invention, showing an example of applying the configuration of the invention to a spline-structured MOS transistor.

The MOS transistor includes a first gate electrode group 1 having a plurality of gate electrodes 1a and 1b formed on a semiconductor substrate to be away from each other at first equal spacings (a); a second gate electrode group 2 having a plurality of gate electrodes 2a and 2b formed on the semiconductor substrate to be away from each other at the first equal spacings (a); and a source contact portion 2 formed between the first and second gate electrode groups to be away the first or second gate electrode group at a second spacing (b). The MOS transistor further includes source regions 3 for electrically interconnecting the first gate electrode group and the source contact portion. These source

regions 3 are connected to each other at one end of the first gate electrode group, and separated from each other by trench gates 1a and 1b at the other end of the first gate electrode group. Preferably, the spacings (b) are greater than the spacings (a).

According to the invention, one source contact 2 has a plurality of trench gates. In addition, the source contact 2 is set as an electrode drawn from a source electrode 4 formed on an upper layer. Since the source contact is a drawn electrode, formation of a source region in one place will eliminate the necessity of forming such regions on the full surface of the semiconductor substrate.

Fig. 6 is a plan view showing a case of applying the configuration of the invention to an offset mesh-structured MOSFET. The MOSFET includes a first gate electrode group 18 having a plurality of gate electrodes 18a formed on a semiconductor substrate to be away from each other at first equal spacings; a second gate electrode group 18 having a plurality of gate electrodes 18b formed on the semiconductor substrate to be away from each other at the first equal spacings; and a source contact portion 24 formed between the first and second gate electrode groups to be away from the first or the second gate electrode group at a second spacing. The MOSFET further includes source regions 26 for electrically interconnecting the first gate electrode group and the source contact portion. These source regions 26 are connected to each other at one end of the first electrode group, and separated from each other by trench gates 18a and 18b at the other end of the same.

In addition, one end of the trench gate is connected. One source contact has a plurality of trench gates. In the embodiment, an arraying ratio between the trench gates 18 and source contacts 24 is set at 4:1. In other words, one source contact 24 is provided for four trench gates 18. Among these trench gates 18, three trench gates 18a arranged on the left side of the source contact are interconnected for one end, and separated from each other for the other end. In such a separated portion, the source region of each gate is connected

through the source region 26 to the source contact 24. According to the invention, one source contact has a plurality of trench gates.

Furthermore, in the semiconductor device of the invention, all the gate electrodes of the first gate electrode group are used as MOS transistor gates. Thus, even with minimum designing space, a channel region density can be increased. the feature of the power MOS transistor.

The above-described semiconductor device of the present invention finds particular utility implemented as a power MOS transistor. The power MOS transistor is designed to obtain power by interconnecting a number of micro-pattern MOSFET cells in parallel. In general, the power MOS transistor is suited for a high-speed operation because of its fast switching speed, and finds application as a switching power source, a motor control circuit, a wide-band power amplifier, and so on. Compared to the prior art, the present invention achieves a decrease in the number of source contacts and an increase in the number of trench gates for the same unit area. For example, the total area of the conventional device shown in Fig.2 and the total area of the device of the present invention shown in Fig.6 may be the same. In that case, the device of Fig.6 has more room for trench gates in so far as the space (a) is smaller that the space (b). For example, in Fig.5, the space (a) is 0.3 μm, the space (b) is 0.5 μm. The present invention thus features a decrease in the number of source contacts and a concomitant reduction in the number of spaces (b).

Now, specific features of the invention will be described by referring to Figs. 7 to 9, wherein Fig. 7 is a sectional view taken on line 2-2 of Fig. 6, Fig. 8 is a sectional view showing a channel forming region, and Fig. 9 is a perspective view showing the semiconductor device of Fig. 7. A manufacturing process of the power MOSFET of the invention will also be briefly described.

First, as shown in Fig. 7, for example, an N-type epitaxial layer 12 is formed on an N type semiconductor substrate 11. On the surface of this epitaxial layer 12, a double diffused layer composed of a P-type base diffused layer 13 and an N type source diffused layer 14 is formed. Then, an SiO film is formed on the source diffused layer 14, and patterned by a resist. Then, using this as a mask, the SiO film is punched. After the removal of the resist, using the SiO film as a mask, a trench 15 is formed to a depth punching through the base diffused layer 13. In this case, one end of the trenches having trench gates 18a (See Fig. 8) formed are connected to each other, while the other ends thereof are not connected. Thus, a source region 26 is formed in this unconnected portion.

Subsequently, the resist is removed. Then, a gate insulating film 16 is formed on a full surface, and a polysilicon film 17 for a gate electrode is formed on this gate insulating film 16. Then, the polysilicon film 17 is removed until the gate insulating film 16 is exposed, and a trench gate 18 is formed.

Then, to separate the trench gate 18 from a later-described source contact, an interlayer film 19 is formed on a full surface. Then, by using a resist (not shown) formed and patterned on this interlayer film 19 as a mask, the interlayer film 19 is removed, and the resist is removed. Furthermore, a gate insulating film 16, a source diffused layer 14 and a base diffused layer 13 are removed, and contact hole 20 is formed to a depth punching through the source diffused layer. Then, using the interlayer film 19 as a mask, impurity ions are implanted, and a P-type diffused layer 21 is formed in the bottom portion of the contact hole 20 inside the base diffused layer 13. Subsequently, a barrier metal layer 22 is formed, an aluminum film 23 is formed on the barrier metal layer 22, and a source contact 24 is formed.

Thus, as shown in Fig. 7, according to the invention, since one source contact 24 is used for four trench gates 18, an arraying ratio between the trench gates 18 and the source

contacts 24 is set at 4:1. In the other end of the trench gate 18a, an open source connection region 26 is provided. One MOSFET set is formed based on the above arraying ratio, and a number of such MOSFET sets are interconnected in parallel on the semiconductor substrate. One MOSFET set of the embodiment is equivalent to four MOSFET sets of the conventional art.

Further as shown in Fig. 8, when a desired voltage is applied to each of trench gates 18a and 18b, a channel region 25 is formed at the side face of the trench 15. In this case, electric charges passed through the channel region 25 are taken out through the source connection region 26 from the source contact 24 located nearby.

Further as shown in Fig. 9, the source region 26 is connected at one end, and separated at the other end by the trench gate 18a. Now, when a voltage is applied to a drain on the semiconductor substrate, electric charges are carried through the channel region 25 at the side face of the trench gate toward the source contact. Since the source regions 26 are connected to each other, electric charges flowing to the side faces of the four trench gates 18a are passed through the source region 26 to reach the source contact 24. Accordingly, since a number of channel regions can be formed in a given region with a minimum designing space, a channel density can be increased, and the device resistance of the MOSFET can be set low owing to this configuration.

In addition, since one source contact has a plurality of trench gates, the number of trench gate/source contact regions can be reduced. For example, the number of spacings (b) shown in Fig. 5 can be reduced. For the spacing (a) between the trench gates shown in Fig. 5, since alignment shifting is less likely to occur compared with the spacing (b) between the trench gate and the source contact, microfabrication is possible for the MOSFET device. Thus, trench gates greater in number than in the conventional case can be formed with minimum designing space. As a result, more MOSFET sets can be connected in parallel.

According to the embodiment of the invention, the source connection region 26 is provided in the trench gate 18a, and the arraying ratio between the trench gates 18 and the source contacts 24 is set at 4:1. Hence, the area density of the channel region 25 can be increased by about 15 to 20%. As a result, low device resistance can be achieved without any problems including a short-circuit failure between the gate and the source, the leakage of current between the drain and the source, and so on.

The invention should not be limited to the foregoing embodiment. For example, the arraying ratio between the trench gates and the source contacts may be set at, e.g., 3:1 other than 4:1. In addition, as shown in Fig. 10, by keeping the same density of the channel region as that in the conventional case, an arraying ratio between trench gates 27 and source contacts 28 may be set at 2:1. In such a case, since an opening of a source contact hole can be set large, e.g., 1 m, a barrier metal layer can be formed to be thick. Thus, the leakage of current between the drain and the source can be suppressed.

Furthermore, the gate may be formed on the semiconductor substrate irrespective of the trench structure.

As apparent from the foregoing, according to the invention, the channel region density can be increased, and low device resistance can be achieved. Therefore, a high operational speed semiconductor device having low ON resistance can be provided.

While there has been illustrated and described what are presently considered to be preferred embodiments of the present invention, it will be understood by those skilled in the art that various changes and modifications may be made, and equivalents may be substituted for devices thereof without departing from the true scope of the invention. In addition, many modifications may be made to adapt a particular situation or material to the teaching of the present invention without departing from the central scope thereof. Therefore, it is intended that this invention not be limited to the particular embodiment

disclosed, but that the invention include all embodiments falling within the scope of the appended claims.

WHAT IS CLAIMED IS AS NEW AND DESIRED TO BE SECURED BY LETTERS PATENT OF THE UNITED STATES IS:

1. A semiconductor device comprising:

a first electrode gate group having a plurality of gate electrodes formed on a semiconductor substrate to be away from each other at first equal spacings;

source contact having a portion formed separated from a first gate electrode of the first electrode gate group by a second spacing greater than the first spacing; and

source regions for electrically interconnecting the first gate electrode group and the source contact.

2. The semiconductor device of Claim 1, wherein the source regions are connected to each other at one end of the first gate electrode group, and separated from each other at the other end of the first gate electrode group.

3. A semiconductor device comprising:

a first gate electrode group having a plurality of gate electrodes formed on a semiconductor substrate to be away from each other at first equal spacings;

a source contact portion formed separated from the first gate electrode group to be away from the first gate electrode groups at a second spacing; and

source regions for electrically interconnecting the first gate electrode group and the source contact,

wherein the source regions are connected to each other at one end of the first gate electrode group, and separated from each other at the other end of the first gate electrode group.

4. A semiconductor device comprising:

a first gate electrode group having a plurality of gate electrodes formed on a semiconductor substrate to be away from each other at first equal spacings;

a second gate electrode group having a plurality of gate electrodes formed on the semiconductor substrate to be away from each other at the first equal spacings:

a source contact portion between the first and second gate electrode groups to be away from the first and second gate electrode groups at a second spacing; and

source regions for electrically interconnecting the first gate electrode group and the source contact,

wherein the source regions are connected to each other at one end of the first gate electrode group, and separated from each other at the other end of the first gate electrode group.

5. A semiconductor device according to claim 4, wherein the gate electrodes of the first group are connected to each other at the other end.

6. A semiconductor device according to claim 4, wherein the first and second gate electrode groups are formed in trench structures.

7. A semiconductor device according to claim 4, wherein each of the source regions is a diffused layer formed on the semiconductor substrate.

8. A semiconductor device according to claim 4, wherein the source contact and the first gate electrode group constitute one MOS transistor.

9. A semiconductor device according to claim 4, further comprising a source electrode on the semiconductor substrate,

wherein the source contact portion is an electrode drawn from the source electrode.

10. A semiconductor device according to claim 4, wherein all the gate electrodes of the first gate electrode group are used as gates for a MOS transistor.

11. A semiconductor device comprising:

a first gate electrode group having a plurality of gate electrodes formed on a semiconductor substrate to be away from each other at first equal spacings;

a second gate electrode group having a plurality of gate electrodes on the semiconductor substrate to be away from each other at the first equal spacings;

a third gate electrode group having a plurality of gate electrodes formed on the substrate to be away from each other at the first equal spacings;

a first source contact portion formed between the first and second gate electrode groups to be away from the first and second gate electrode groups at a second spacing;

a second source contact portion formed between the second and third gate electrode groups to be away from one selected from the second and third gate electrode groups at the second spacing;

first source regions which electrically interconnect the first gate electrode group and the first source contact portion; and

second source regions which electrically interconnect the second gate electrode group and the second source contact,

wherein the first source regions are connected to each other at one end of the first gate electrode group and are separated from each other at the other end of the first gate

electrode group, and the second source regions are connected to each other at one end of the second gate electrode group and are separated from each other at the other end of the second gate electrode group.

12. A semiconductor device according to claim 11, wherein the first and second gate electrode groups are connected to each other at the other end.

13. A semiconductor device according to claim 11, wherein the second source regions are connected to each other at one end of the second gate electrode group, and separated from each other at the other end of the second gate electrode group.

14. A semiconductor device according to claim 11, wherein the first and second gate electrode groups are formed in trench structures.

15. A semiconductor device according to claim 11, wherein each of the first and second source regions is a diffused layer formed on the semiconductor substrate.

16. A semiconductor device according to claim 11, wherein the first source contact portion and the first gate electrode group constitute one MOS transistor, and the second source contact portion and the second gate electrode group constitute another MOS transistor.

17. A semiconductor device according to claim 11, wherein each of the first and second source contact portions is an electrode drawn from a source electrode, and these portions are connected to each other.

18. A semiconductor device according to claim 11, wherein all the gate electrodes of the first and second gate electrode groups are used as gates for MOS transistors.

19. A semiconductor device according to claim 11, wherein the second source regions are connected to each other at one end of the second gate electrode group, and separated from each other at the other end of the second gate electrode group.

20 A semiconductor device according to claim 11, wherein the second spacing is greater than the first spacing.

ABSTRACT OF THE DISCLOSURE

A semiconductor device, and particularly an MOS transistor device, wherein in order to increase a channel region density and to achieve a low resistance of a transistor device there is provided a first gate electrode group having a plurality of gate electrodes formed on a semiconductor substrate to be away from each other at first equal spacings, a second gate electrode group having a plurality of gate electrodes formed on the semiconductor substrate to be away from each other at the first equal spacings, a source contact portion formed away from the first or the second gate electrode group at a second spacing, and source regions for electrically interconnecting the first gate electrode group and the source contact. The source regions are connected to each other at one end of the first gate electrode group, and separated at the other end of the first gate electrode group. In addition, the gate electrodes of the first group are connected each other at the other end. The second spacing is greater than the first spacing.

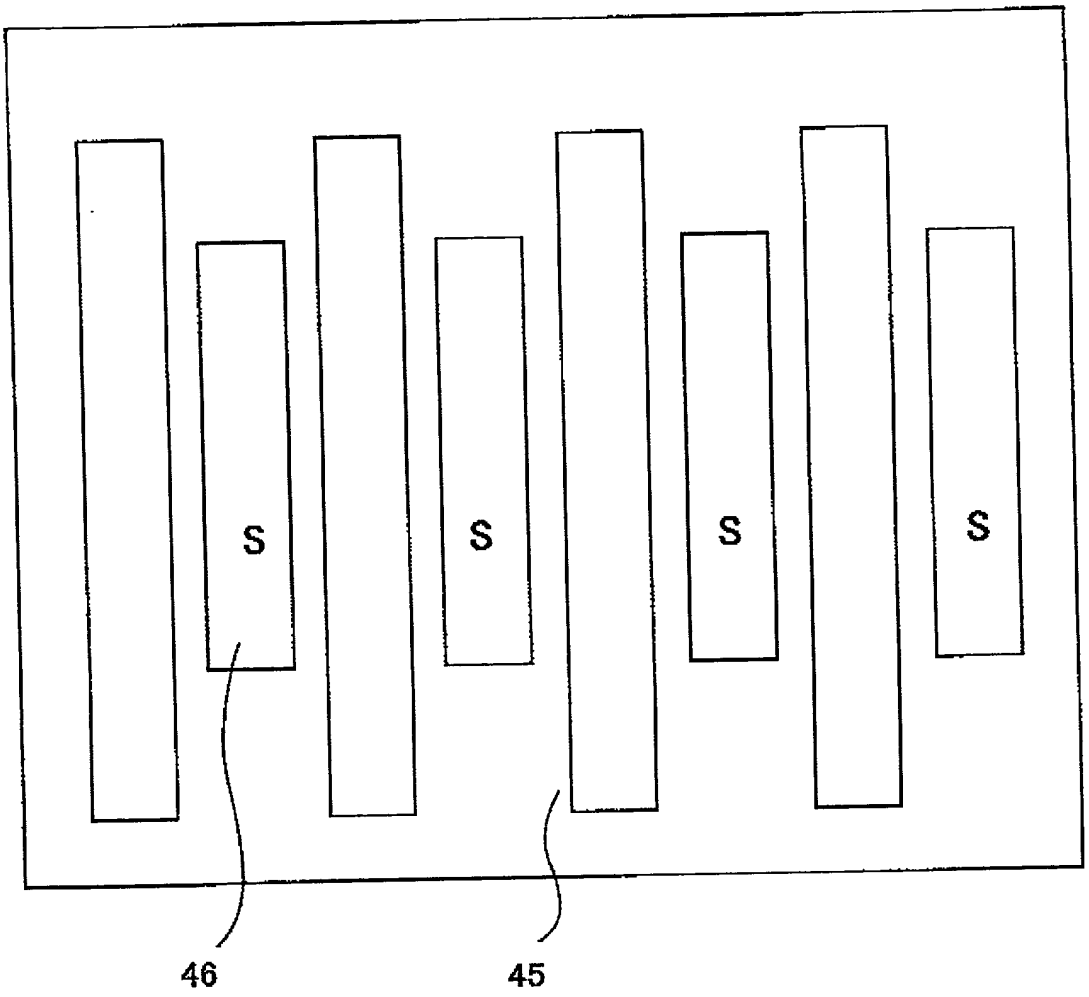

FIG. 1 (PRIOR ART)

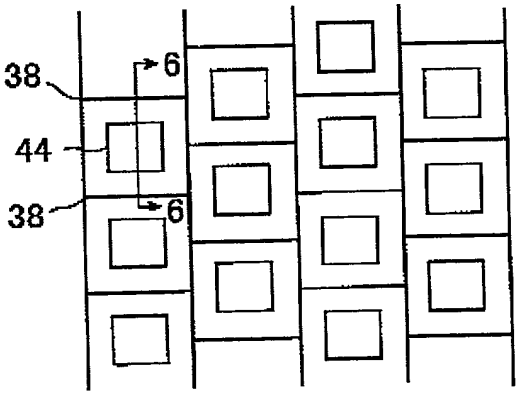

FIG. 2 (PRIOR ART)

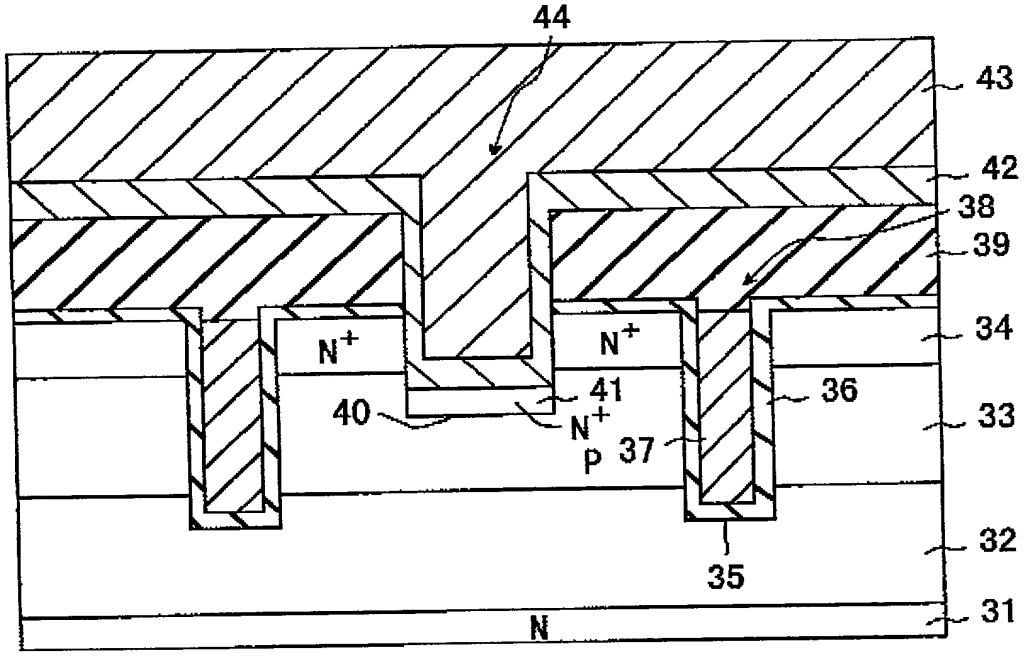

FIG. 3 (PRIOR ART)

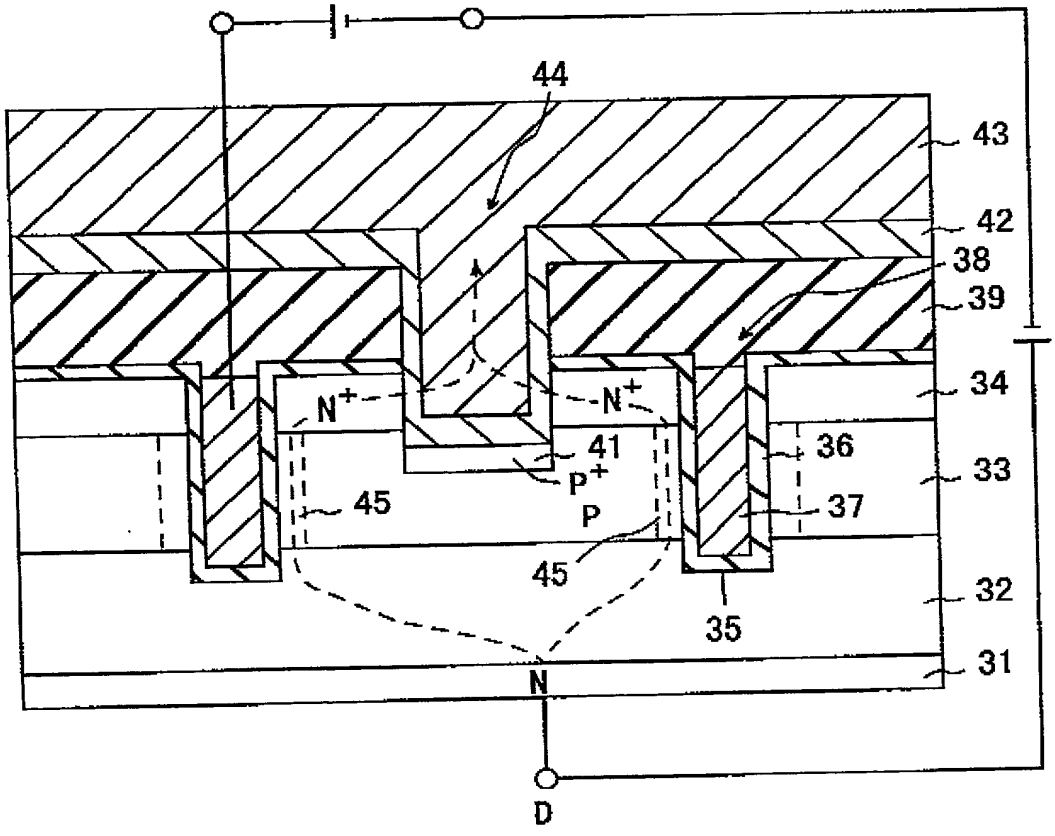

FIG. 4 (PRIOR ART)

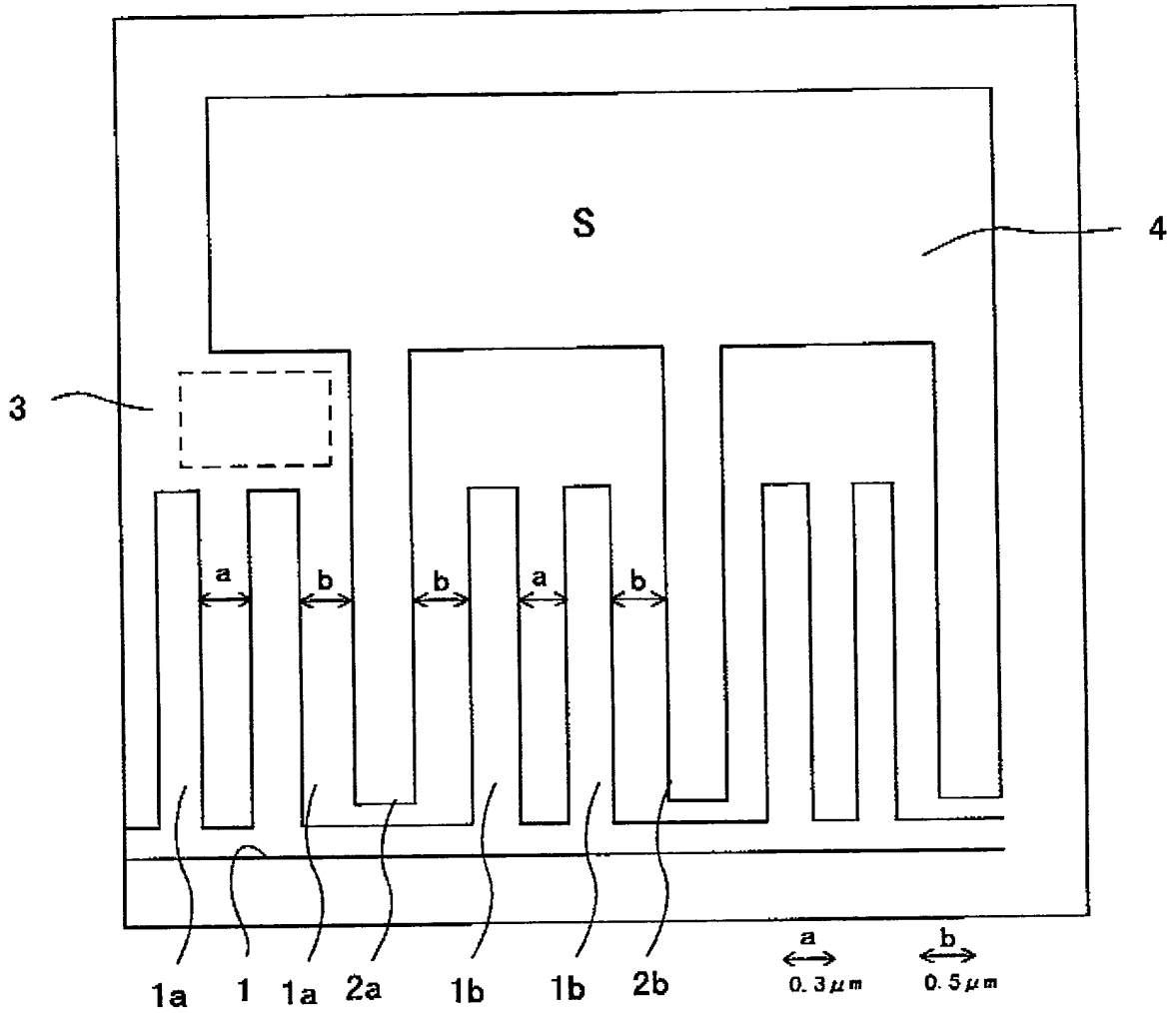

FIG. 5

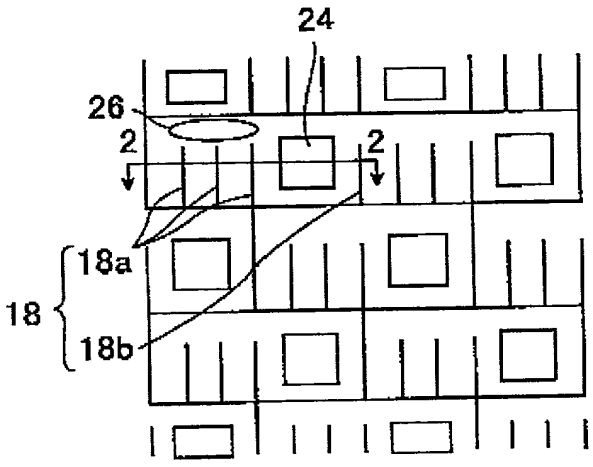

FIG. 6

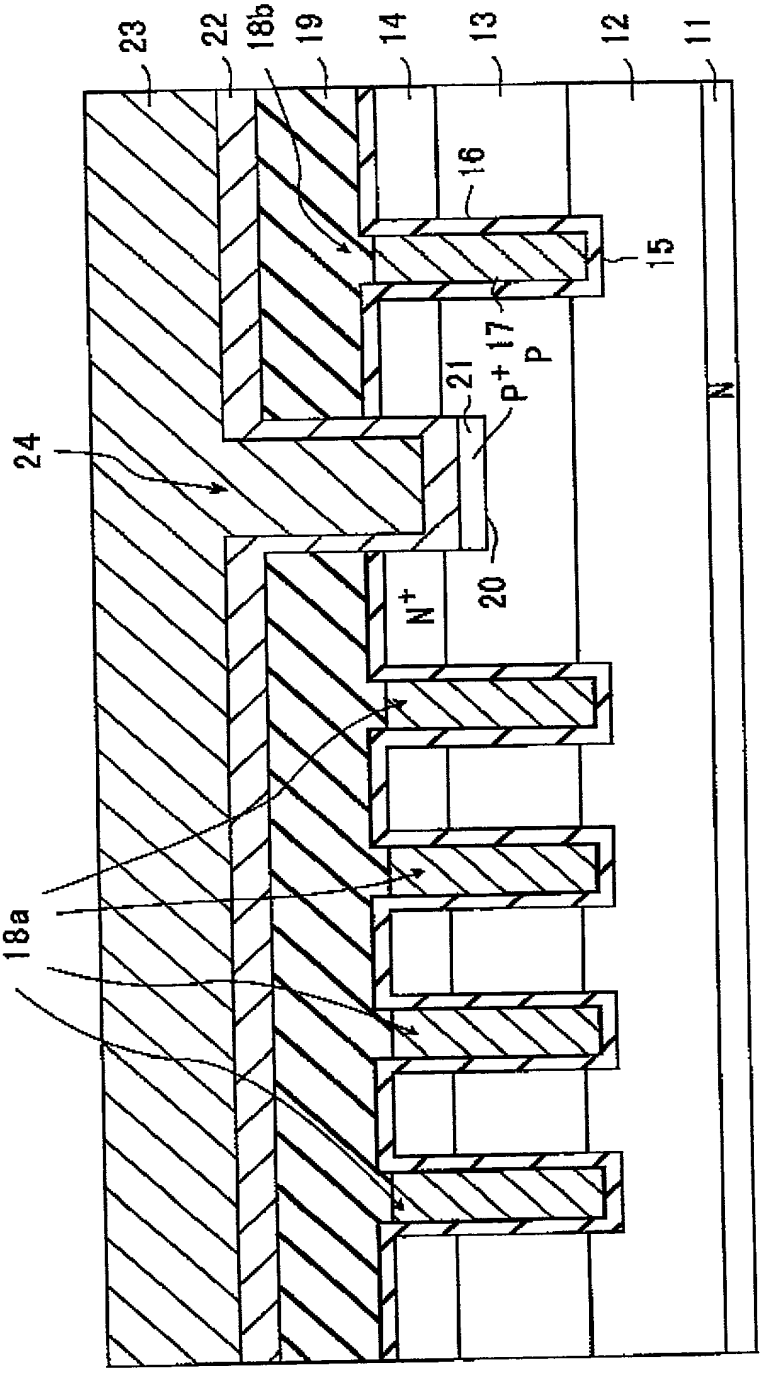

FIG. 7

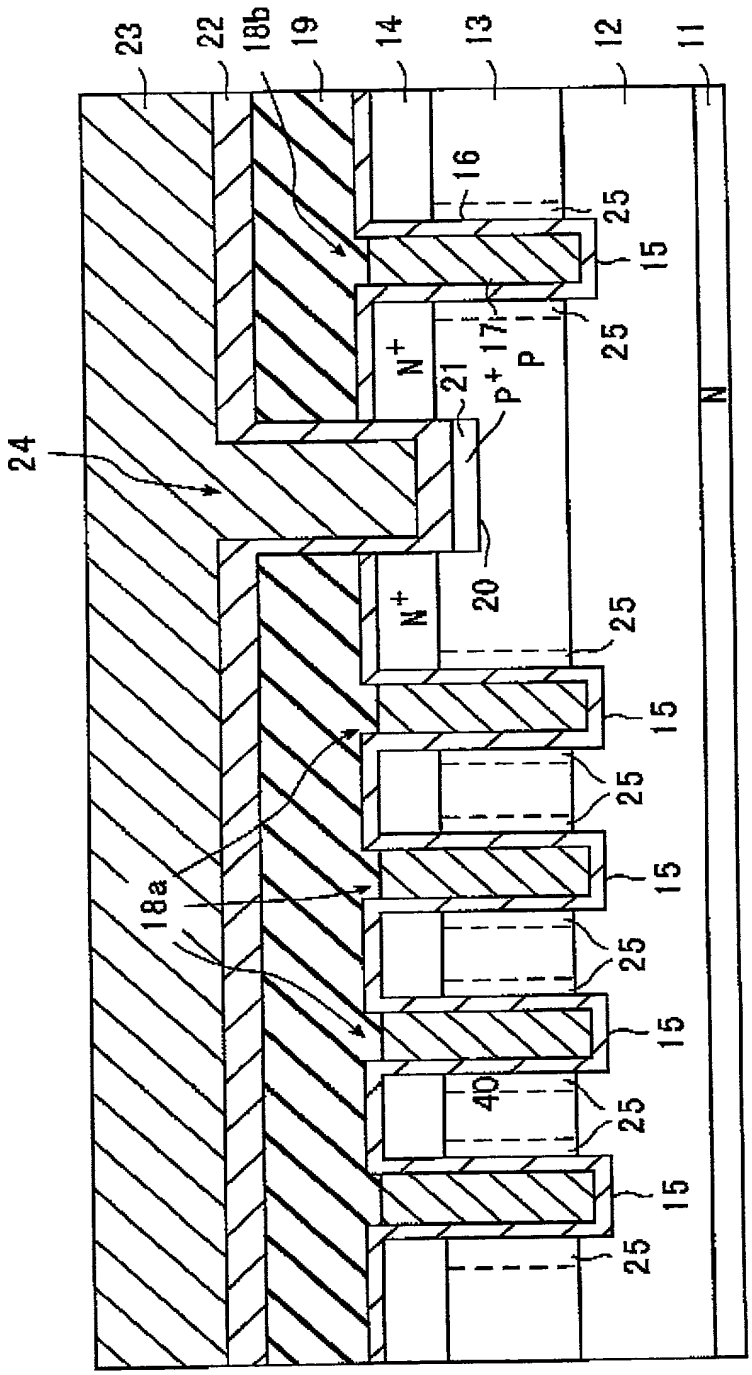

FIG. 8

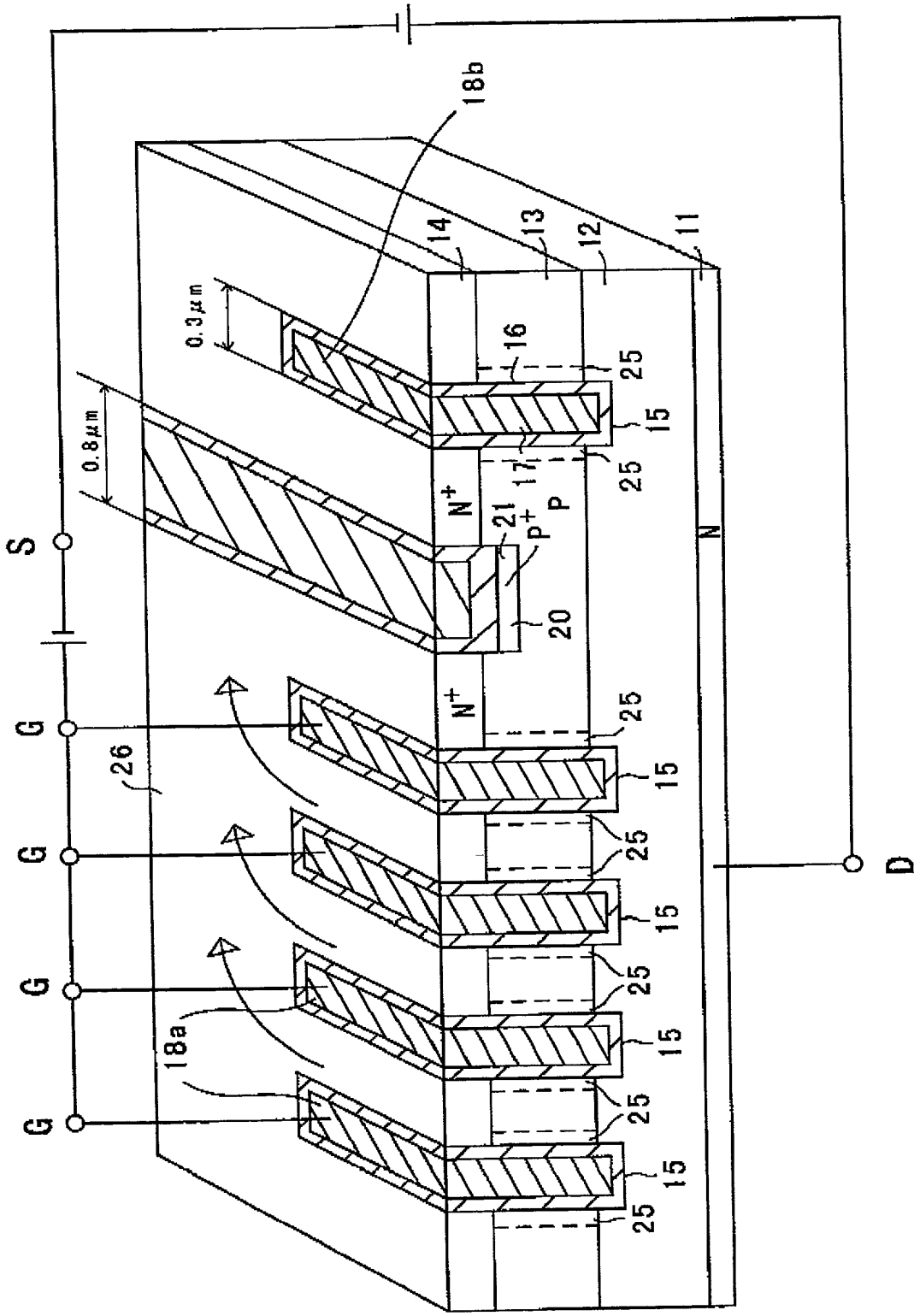

FIG. 9

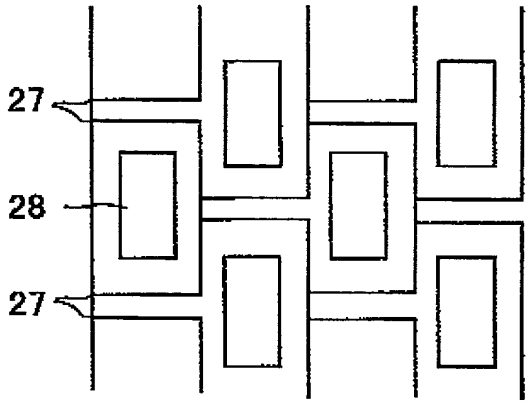

FIG. 10

Docket No. **197226US-2TTC**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: **NOBORU MATSUDA ET AL**

FILING DATE: **Herewith**

FOR: **POWER MOS TRANSISTOR HAVING TRENCH GATE**

LIST OF INVENTORS' NAMES AND ADDRESSES

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A declaration containing all the necessary information will be submitted at a later date.

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